**Cell Description:**This is a standard tristate inverter cell. This cells functionality is described by the following Boolean equation:

**Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **P\_EN** | **N\_EN** | **Y** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | Z |
| 0 | 1 | 1 | Z |
| 1 | 0 | 0 | Z |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | Z |
| 1 | 1 | 1 | 0 |

**Behavioral Verilog:**//Verilog HDL for "Lib6710\_06", "TRINV" "behavioral"

module TRINV ( Y, A, N\_EN, P\_EN );

input A;

input N\_EN;

output Y;

input P\_EN;

assign Y = (N\_EN & ~P\_EN) ? ~A : 1'bz;

specify

(A => Y) = (1.0, 1.0);

(N\_EN => Y) = (1.0, 1.0);

(P\_EN => Y) = (1.0, 1.0);

endspecify

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| TRINV | 27.0 | 7.2 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min.** | **Max.** |
| TRINV |  |  |

**Logic Symbol:**

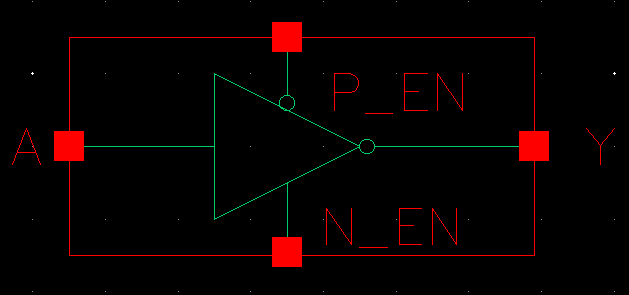
****

Figure 1: Symbol View for the TRINV cell

**CMOS Schematic:**

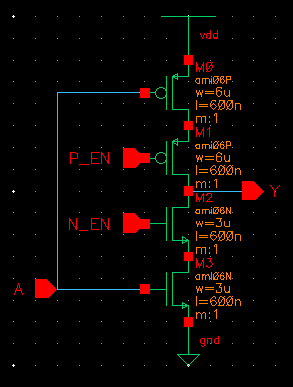
****

Figure 2: CMOS Schematic for TRINV cell.

**CMOS Layout:**

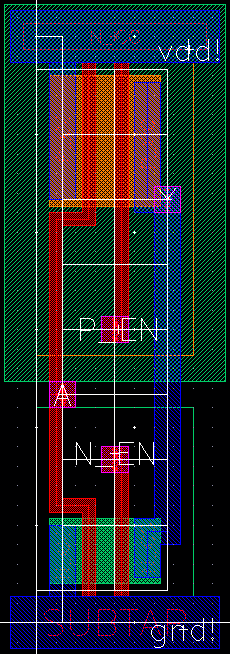
****

Figure 3: CMOS layout for TRINV cell.